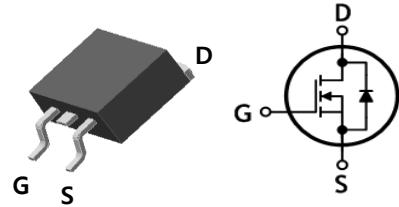


N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=700V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.19\Omega$ (Max.)
- Ultra low gate charge: $Q_g=20nC$ (Typ.)
- RoHS compliant device
- 100% avalanche tested

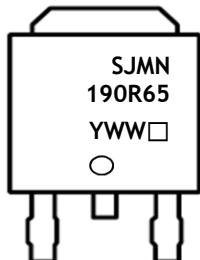


TO-263 (D2-PAK)

Ordering Information

Part Number	Marking	Package
SJMN190R65B	SJMN190R65	TO-263

Marking Information



Column 1: Manufacturer
 Column 2: Production Information
 e.g.) YWW□
 - YWW: Data Code (year, week)
 - □: Management Code

Absolute maximum ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		650	V
Gate-source voltage	V_{GSS}		± 30	V
Drain current (DC) ^(Note 1)	I_D	$T_c=25^{\circ}C$	20	A
		$T_c=100^{\circ}C$	12.6	A
Drain current (Pulsed) ^(Note 1)	I_{DM}		80	A
Single pulsed avalanche energy ^(Note 2)	E_{AS}		265	mJ
Repetitive avalanche current ^(Note 1)	I_{AR}		7	A
Repetitive avalanche energy ^(Note 1)	E_{AR}		15	mJ
Power dissipation	P_D		150	W
Diode dv/dt ruggedness ^(Note 3)	dv/dt		15	V/ns
MOSFET dv/dt ruggedness ^(Note 4)	dv/dt		50	V/ns
Junction temperature	T_J		150	$^{\circ}C$
Storage temperature range	T_{stg}		-55~150	$^{\circ}C$

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 0.83	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=V_{GS}$	2	3	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=650V, T_J=125^\circ C$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 30V$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$	-	0.155	0.19	Ω
Internal gate resistance	R_g	f=1MHz, Open drain	-	18	-	Ω
Input capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	-	1533	-	pF
Output capacitance	C_{oss}		-	846	-	
Reverse transfer capacitance	C_{rss}		-	23	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	$V_{DS}=350V, I_D=20A, R_G=25\Omega$	-	25	-	ns
Rise time (Note 5)	t_r		-	21	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	60	-	
Fall time (Note 5)	t_f		-	4	-	
Total gate charge (Note 6)	Q_g	$V_{DS}=400V, V_{GS}=10V, I_D=10A$	-	36	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	10	-	
Gate-drain charge (Note 6)	Q_{gd}		-	10	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_s	Integral reverse diode in the MOSFET	-	-	20	A
Source current (Pulsed)	I_{SM}		-	-	80	A
Forward voltage	V_{SD}	$V_{GS}=0V, I_s=20A$	-	-	1.2	V
Reverse recovery time (Note 5, 6)	t_{rr}	$I_s=20A, V_{GS}=0V, dI_s/dt=100A/us$	-	383	-	ns
Reverse recovery charge (Note 5, 6)	Q_{rr}		-	4.6	-	uC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. L=10mH, $I_{AS}=7A$, $V_{DD}=50V$, Starting $T_J=25^\circ C$
3. $I_s \leq 20A$, $V_{DS} \leq 400V$, $dI_s/dt \leq 100A/us$, $T_J=25^\circ C$
4. $V_{DS} \leq 400V$, $I_s \leq 20A$
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

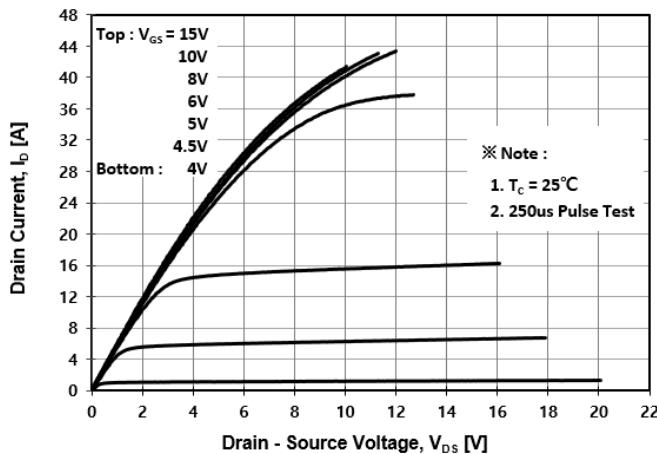


Fig. 2 Typical Transfer Characteristics

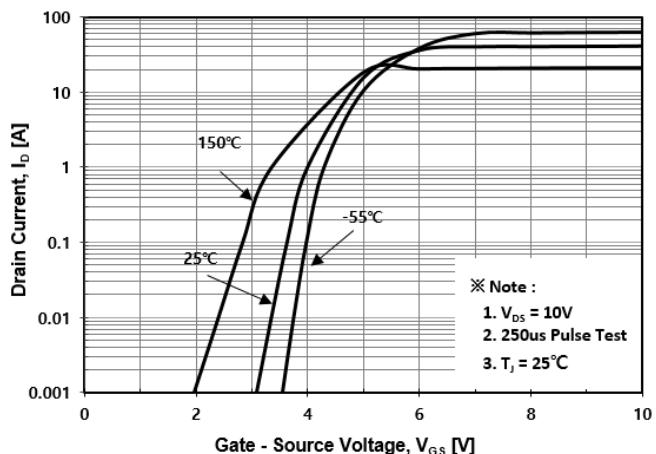


Fig. 3 On-Resistance Variation with Drain Current and Gate Voltage

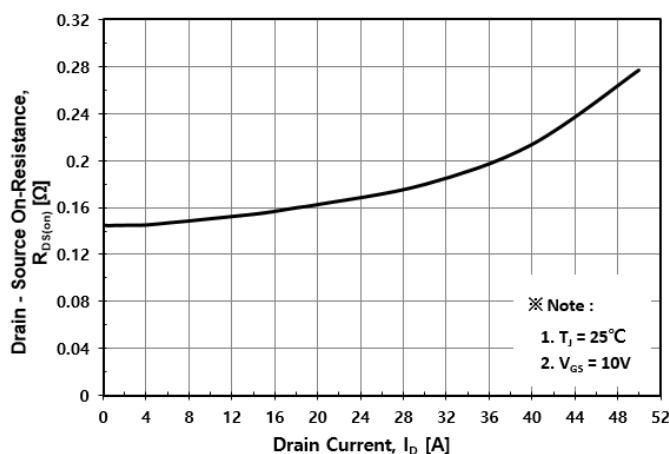


Fig. 4 Body Diode Forward Voltage Variation with Source Current

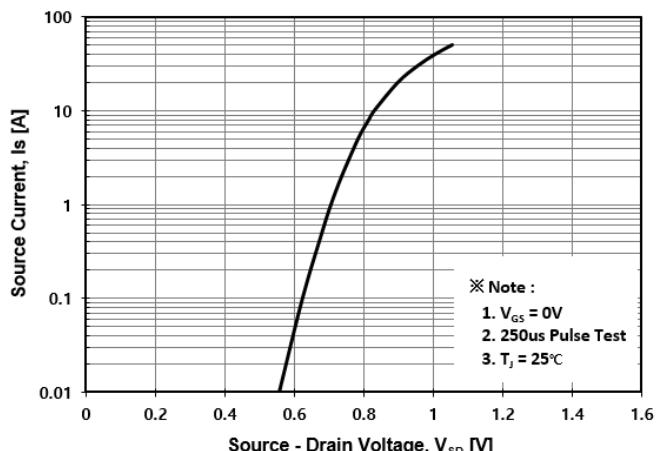


Fig. 5 Typical Capacitance Characteristics

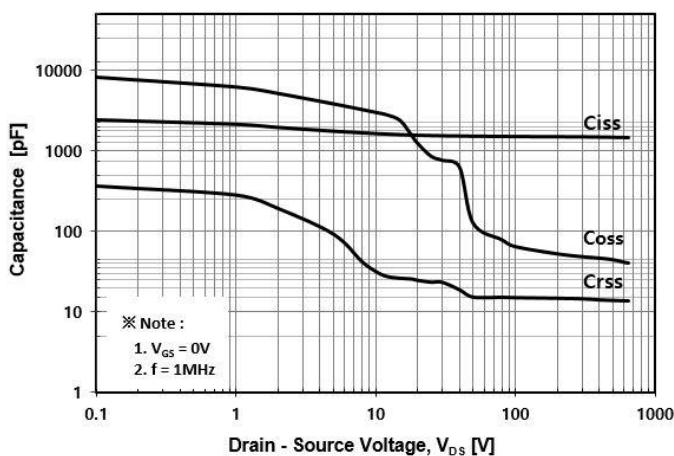
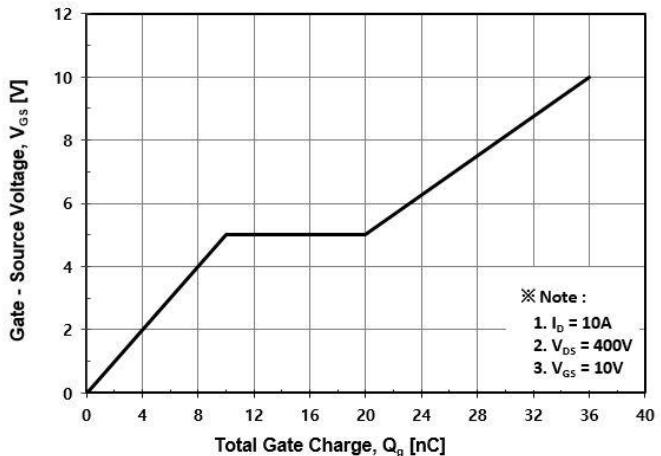


Fig. 6 Typical Total Gate Charge Characteristics



Typical Electrical Characteristics Curves

Fig. 7 Breakdown Voltage Variation vs. Temperature

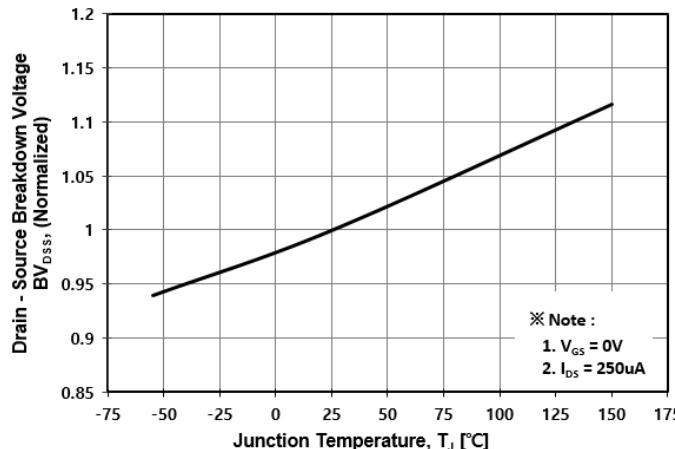


Fig. 8 On-Resistance Variation vs. Temperature

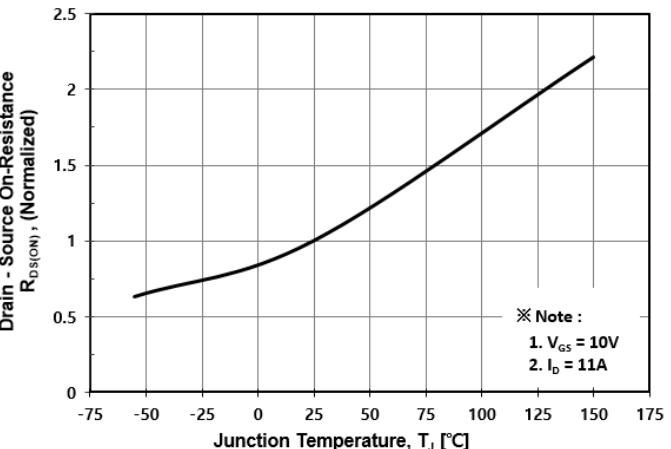


Fig. 9 Maximum Drain Current vs. Case Temperature

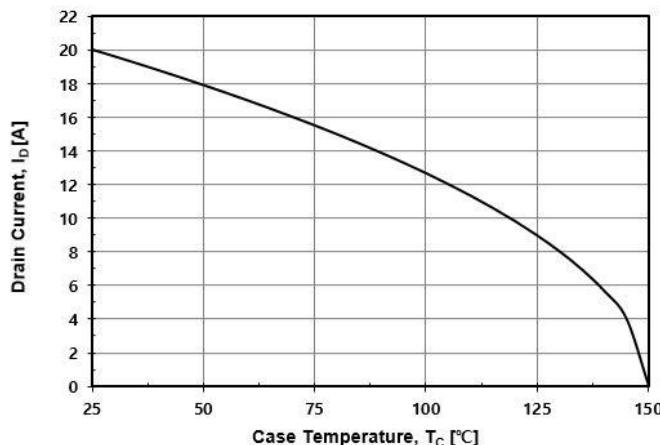


Fig. 10 Maximum Safe Operating Area

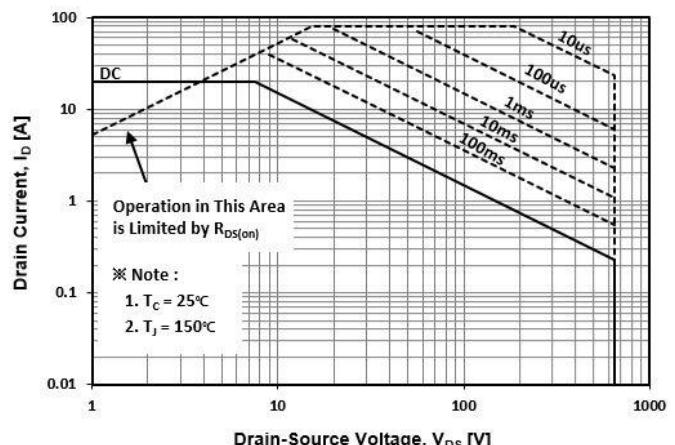


Fig. 11 Transient Thermal Impedance

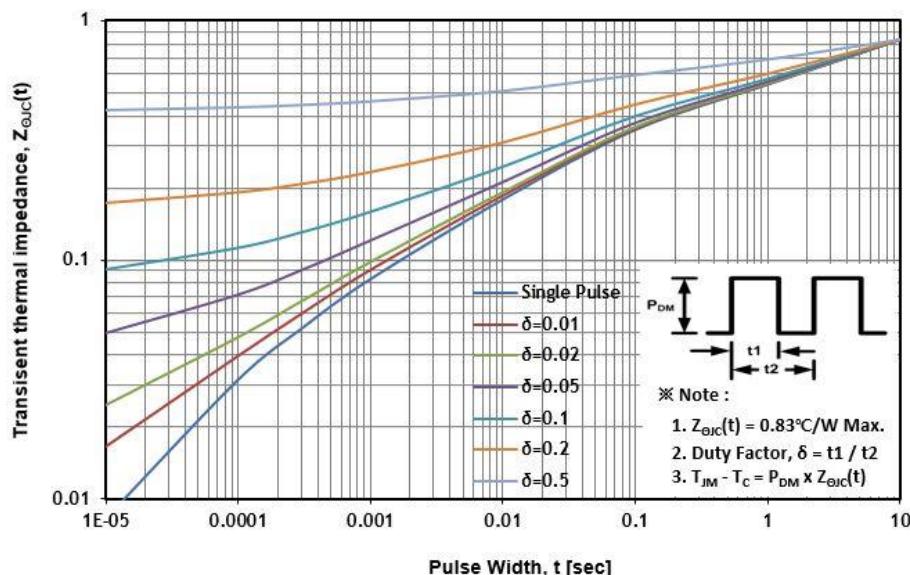


Fig. 12 Gate Charge Test Circuit & Waveform

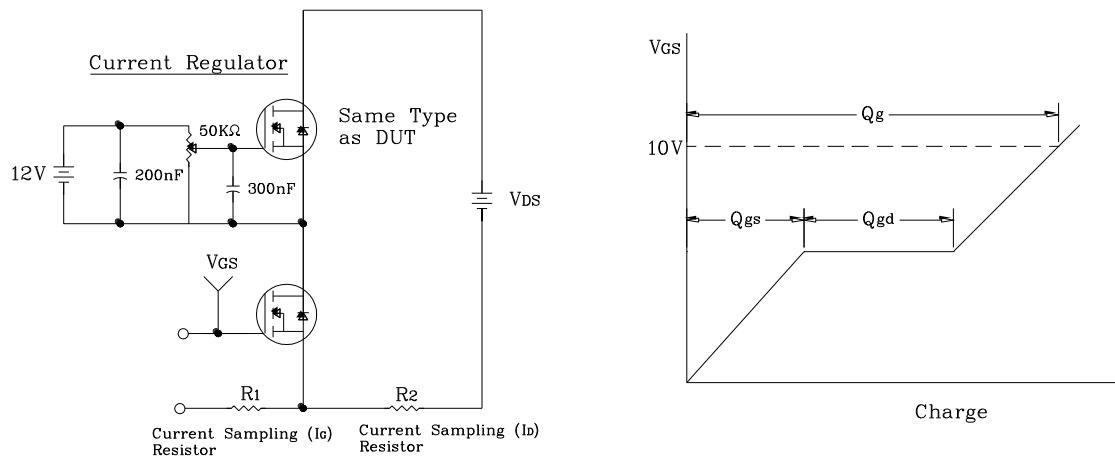


Fig. 13 Resistive Switching Test Circuit & Waveform

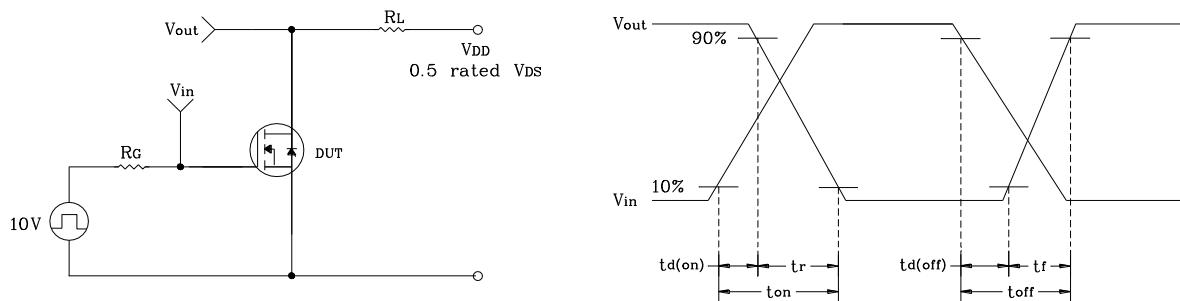


Fig. 14 E_{AS} Test Circuit & Waveform

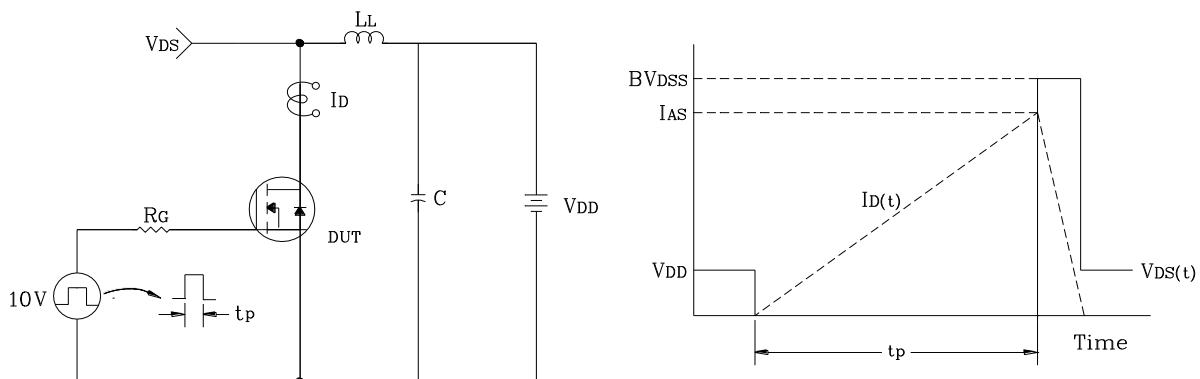
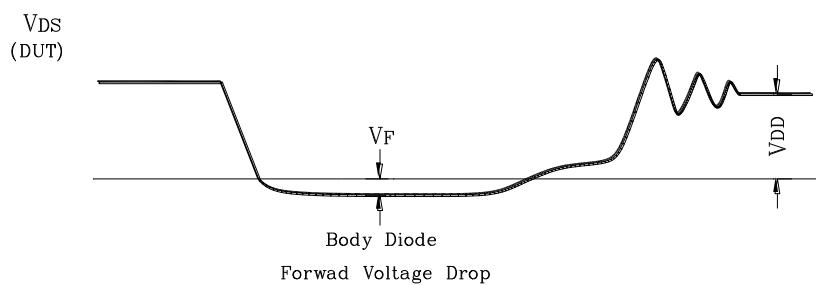
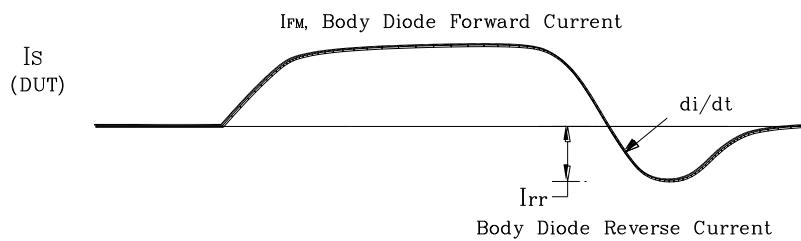
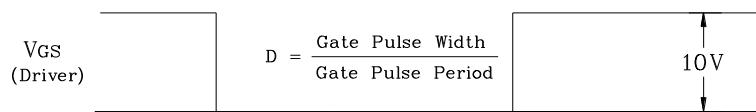
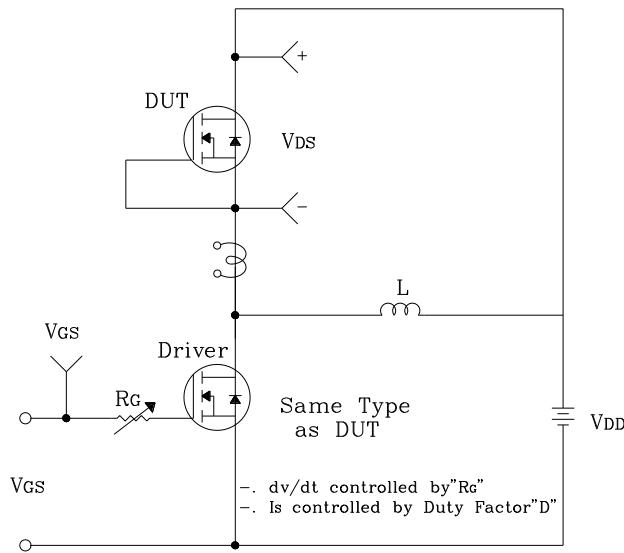
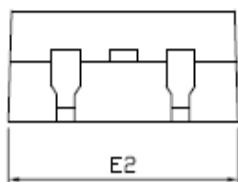
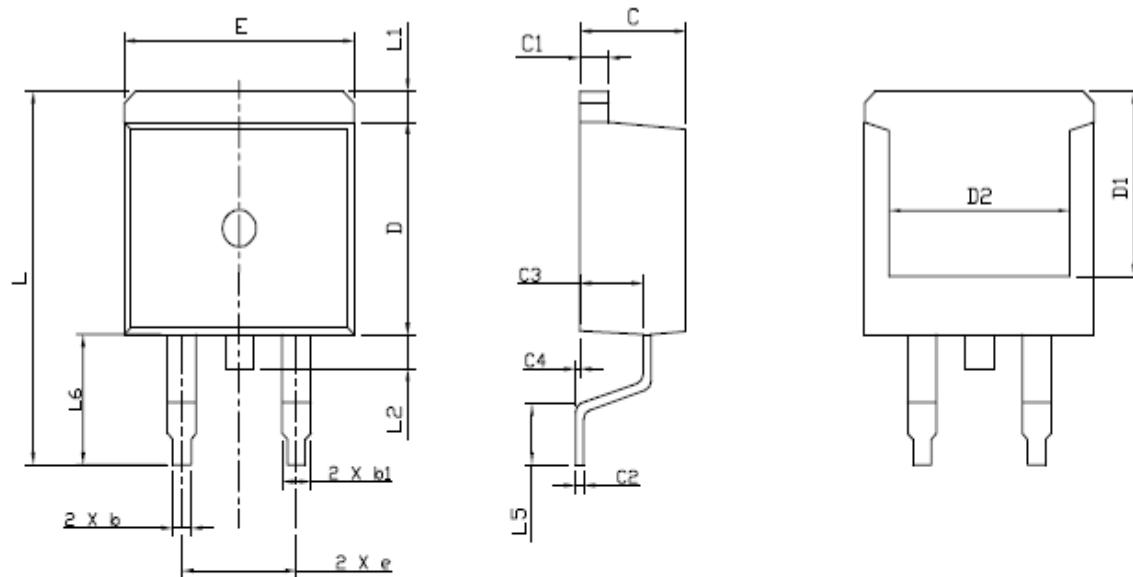


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions

SYMBOL	MILLIMETERS		
	MINIMUM	NOMINAL	MAXIMUM
b	0.73	0.80	0.87
b1	1.20	1.27	1.34
C	4.38	4.48	4.58
C1	1.23	1.30	1.37
C2	0.43	0.50	0.57
C3	2.25	2.40	2.55
C4	0.02	0.10	0.18
D	9.10	9.20	9.30
D2	7.90	8.00	8.10
E	9.78	9.88	9.98
e	4.98	5.08	5.18
E2	9.75	9.90	10.05
L	14.95	15.20	15.45
L1	1.15	1.30	1.45
L2	1.50	1.60	1.70
L5	2.25	2.40	2.55
L6	4.60	4.80	5.00

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