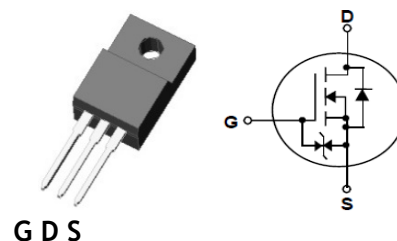


700V N-Channel Super Junction MOSFET

Features

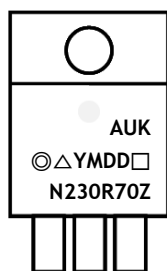
- Drain-Source voltage: $V_{DS}=750V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.2\Omega$ (Typ.)
- Very Low FOM ($R_{DS(on)} \times Q_g$)
- 100% avalanche tested
- Built-in ESD Diode



Ordering Information

Part Number	Marking	Package
SJMN230R70ZF	N230R70Z	TO-220F-3L

Marking Information



Column 1: Manufacturer Logo
Column 2: Production Information

- ◎: Management Code
- △: Machine Code
- YMDD: Date Code Marking (Year, Monthly, Daily)
- □: Factory Management Code

Column 3: Device Code

Absolute maximum ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	700	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current (DC) *	I_D	$T_C=25^{\circ}C$	16
		$T_C=100^{\circ}C$	10.1
Drain current (Pulsed) *	I_{DM}	48	A
Single pulsed avalanche energy (Note 2)	E_{AS}	228	mJ
Single pulsed avalanche current (Note 2)	I_{AS}	2.3	A
Repetitive avalanche energy (Note 1)	E_{AR}	3.3	mJ
Power dissipation	P_D	33	W
Gate to source ESD (Human Body Model)	$V_{ESD(G-S)}$	2000	V
Junction temperature	T_J	150	$^{\circ}C$
Storage temperature range	T_{stg}	-55~150	$^{\circ}C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.79	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=1\text{mA}$, $V_{GS}=0$	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=670\mu\text{A}$, $V_{DS}=V_{GS}$	2	-	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=700\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=700\text{V}$, $T_C=150^{\circ}\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 1	μA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5.7\text{A}$	-	0.2	0.23	Ω
Input capacitance	C_{iss}	$V_{DS}=400\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	2078	-	pF
Output capacitance	C_{oss}		-	38	-	
Reverse transfer capacitance	C_{rss}		-	4.4	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=350\text{V}$, $I_D=9.6\text{A}$, $R_G=25\Omega$	-	38	-	ns
Rise time (Note 3,4)	t_r		-	37	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	115	-	
Fall time (Note 3,4)	t_f		-	42	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=560\text{V}$, $V_{GS}=10\text{V}$, $I_D=8.7\text{A}$	-	44	-	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	9	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	16	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	16	A
Source current (Pulsed)	I_{SM}		-	-	48	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=8.7\text{A}$	-	-	1.3	V
Reverse recovery time (Note 3,4)	t_{rr}	$V_R=400\text{V}$, $I_S=8.7\text{A}$, $V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	490	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	2.3	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $I_{AS}=2.3\text{A}$, $L=86\text{mH}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics Curve

Fig. 1 $I_D - V_{DS}$

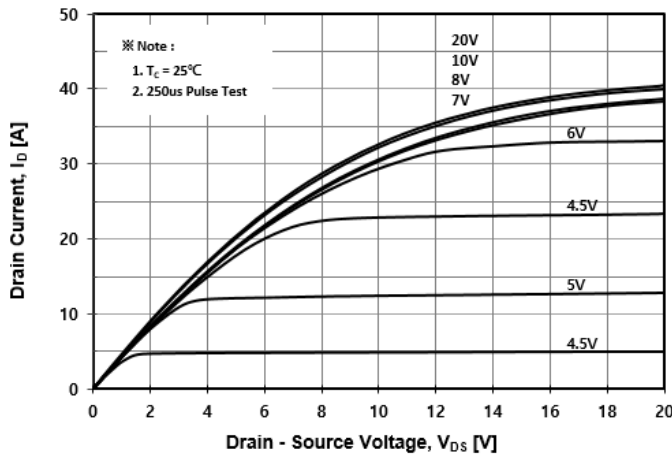


Fig. 2 $I_D - V_{GS}$

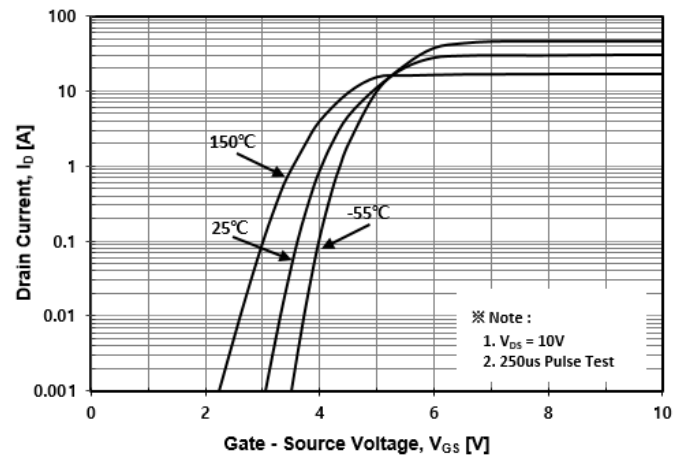


Fig. 3 $R_{DS(ON)} - I_D$

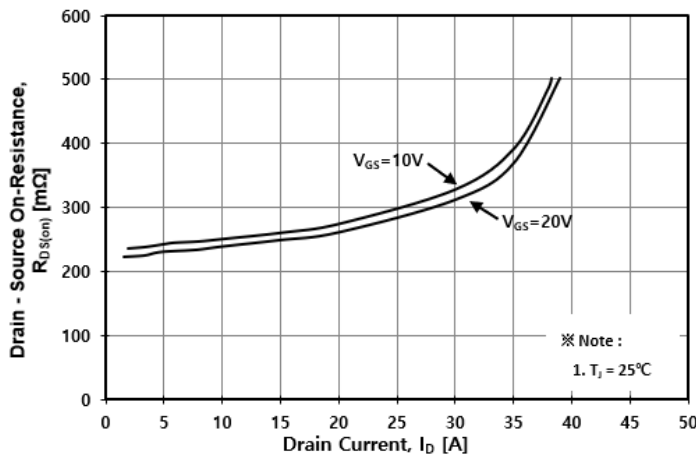


Fig. 4 $I_S - V_{SD}$

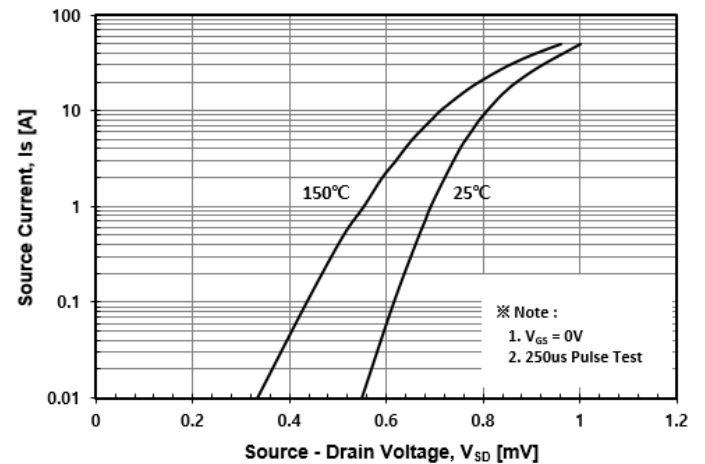


Fig. 5 Capacitance - V_{DS}

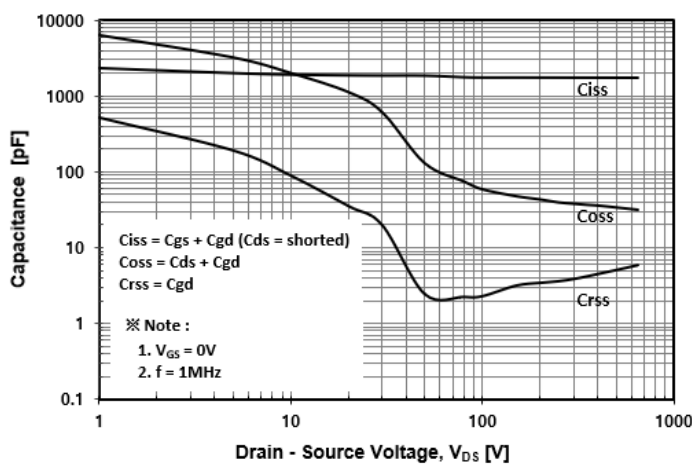
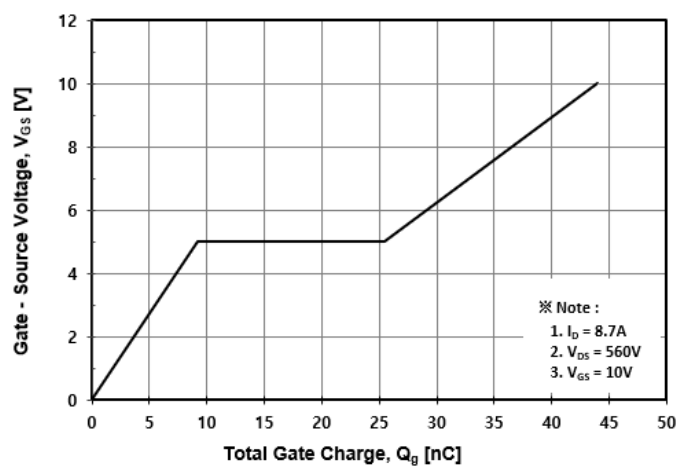


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics Curve (Continue)

Fig. 7 Normalized $BV_{DSS} - T_J$

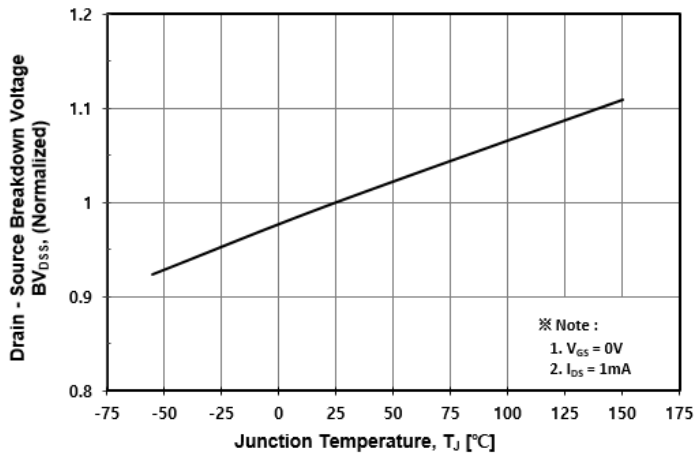


Fig. 8 Normalized $R_{DS(ON)} - T_J$

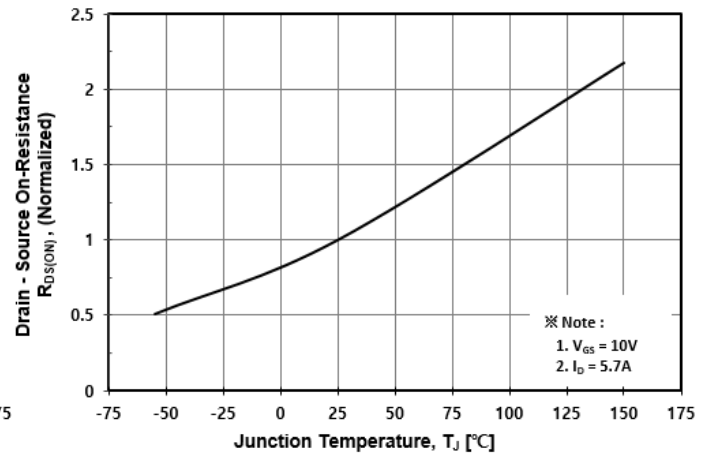


Fig. 9 $I_D - T_C$

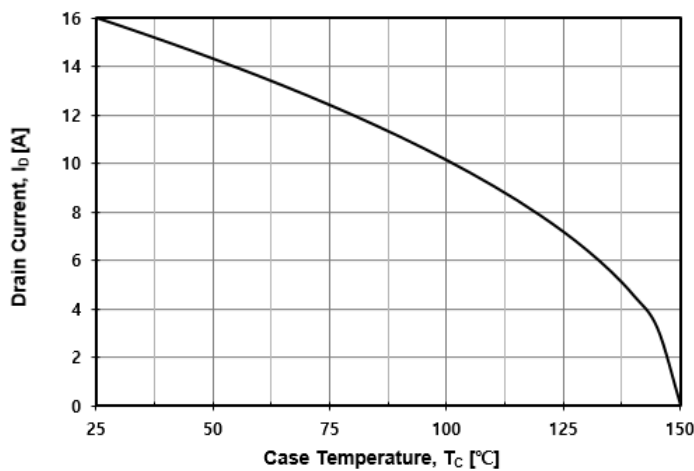


Fig. 10 Safe Operating Area

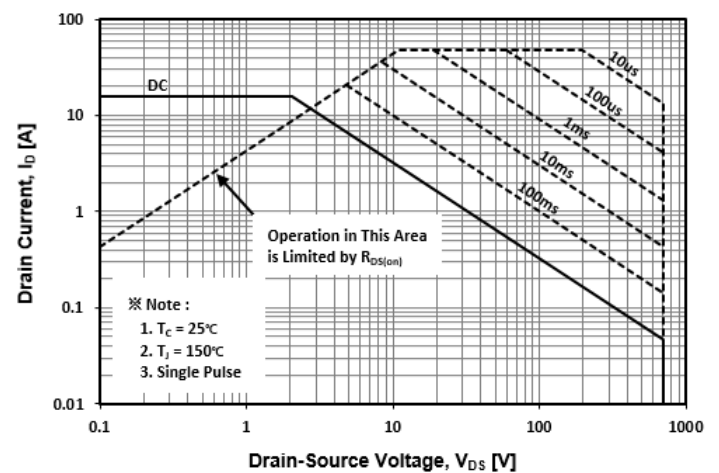


Fig. 11 Maximum Transient Thermal Impedance

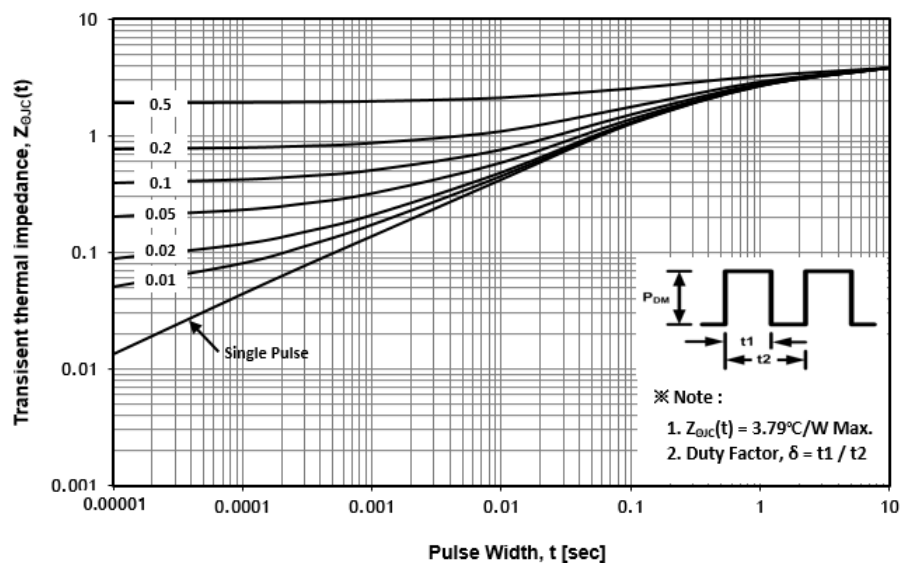


Fig. 12 Gate Charge Test Circuit & Waveform

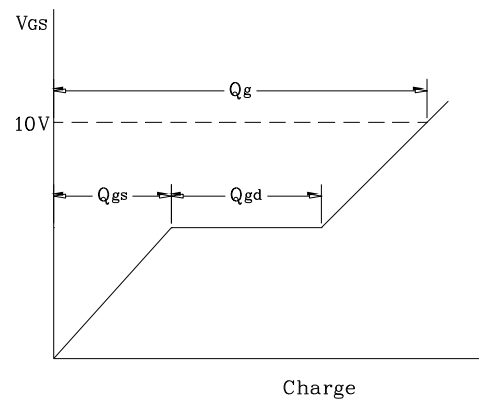
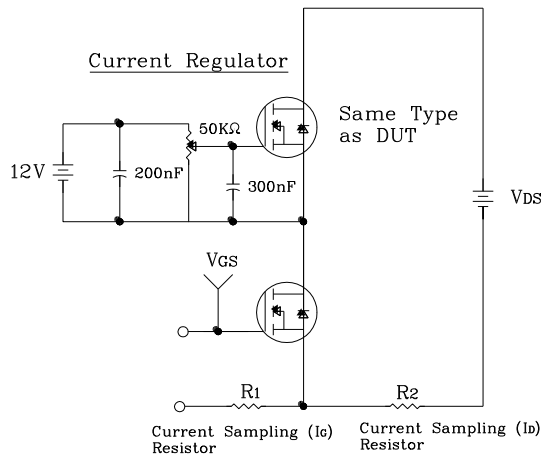


Fig. 13 Resistive Switching Test Circuit & Waveform

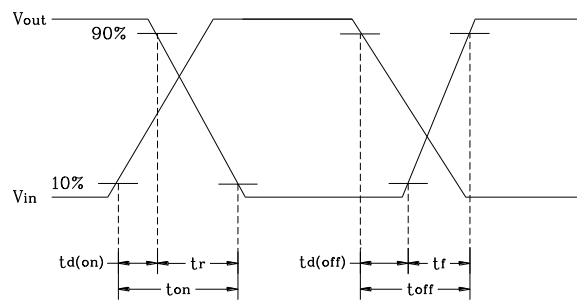
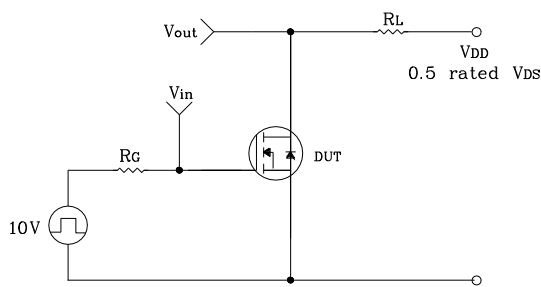


Fig. 14 E_{AS} Test Circuit & Waveform

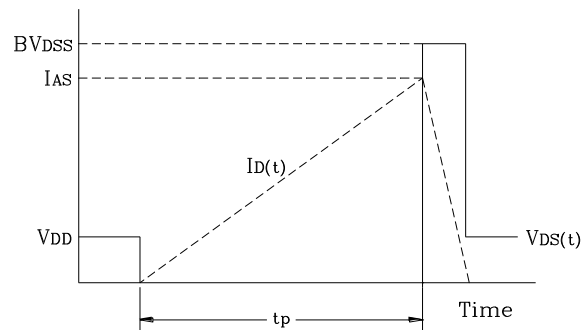
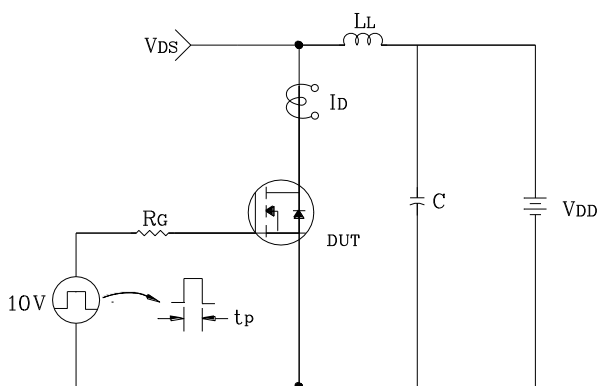
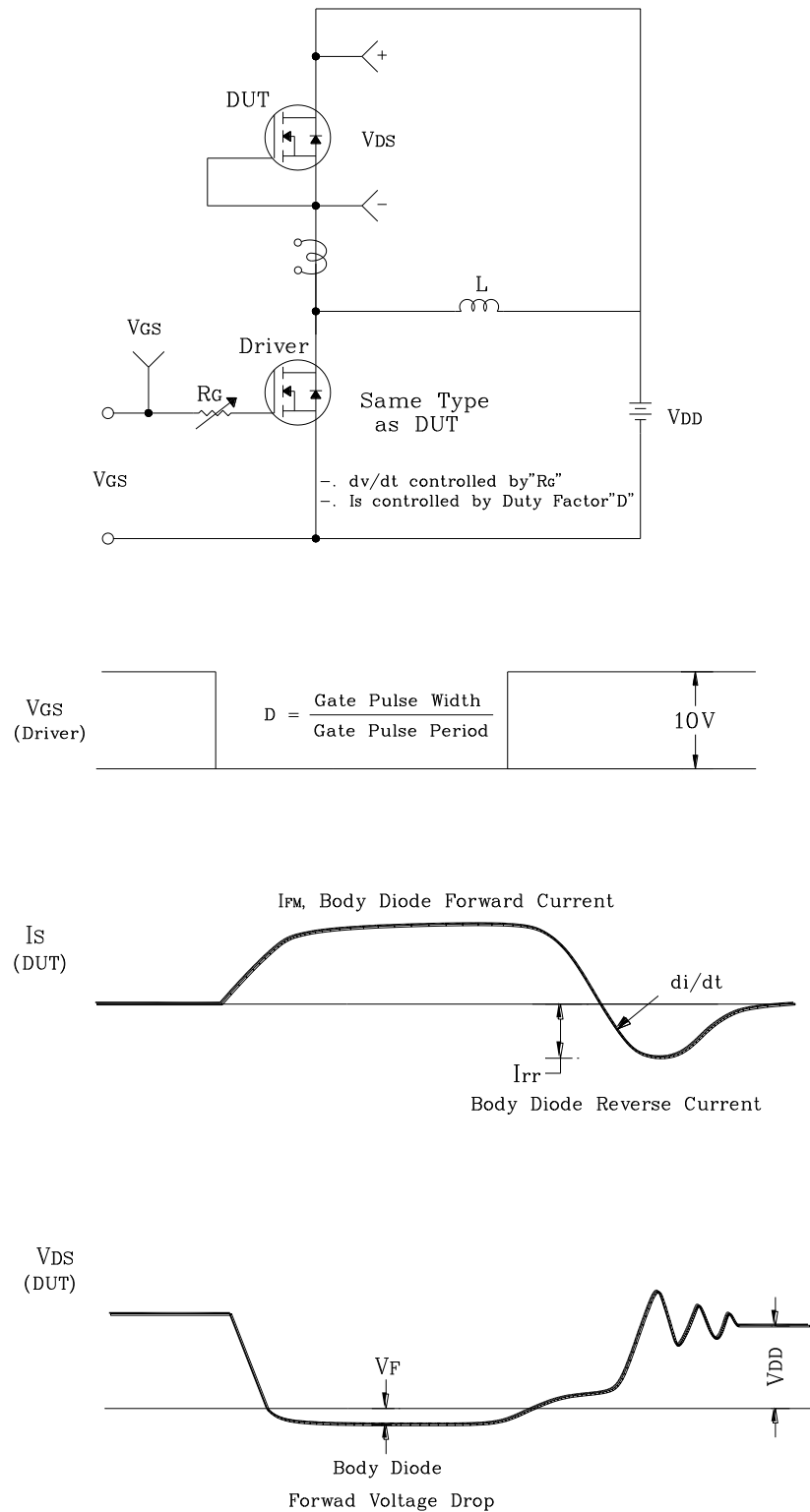
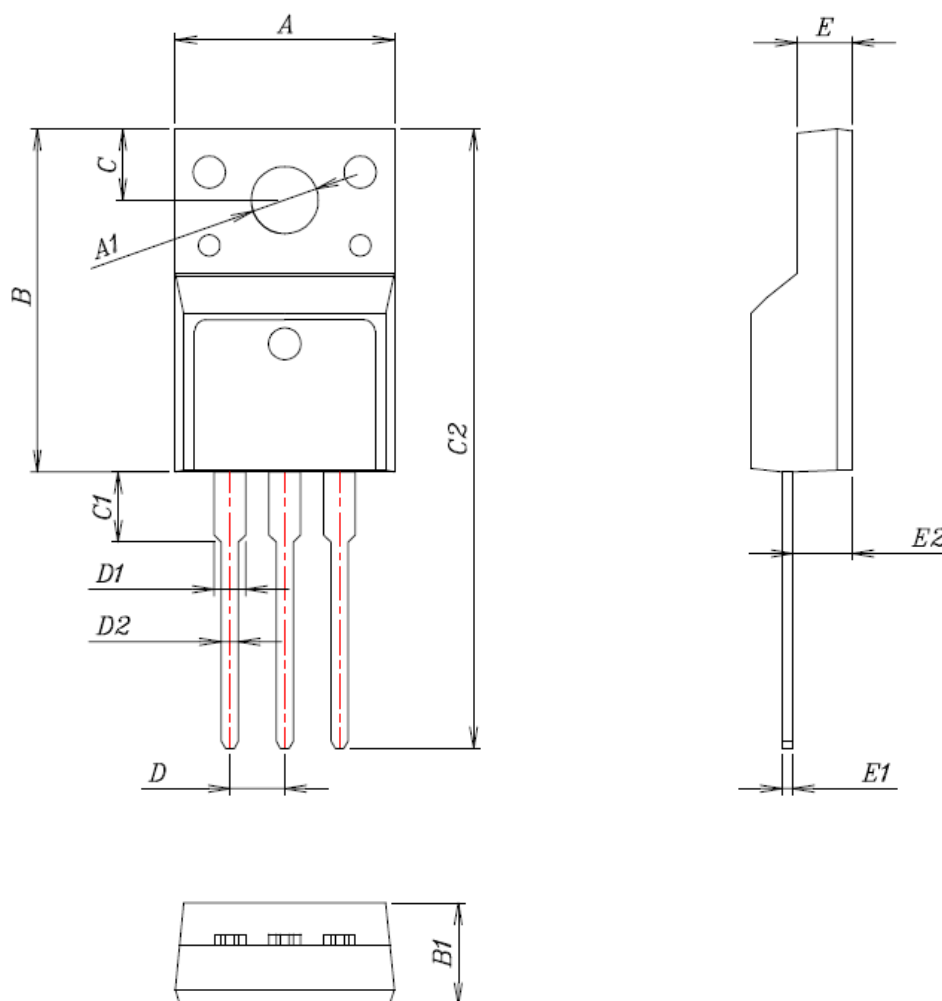


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS
A	10.16±0.30
A1	3.12±0.20
B	15.90±0.50
B1	4.70±0.30
C	3.30±0.25
C1	3.25±0.30
C2	28.70±0.50
D	Typical 2.54
D1	1.47(MAX)
D2	0.80±0.20
E	2.55±0.25
E1	0.50±0.20
E2	2.75±0.30

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